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Design of eFuse OTP IP for Light Sensors Using Single Devices

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Abstract

A light sensor chip requires a small capacity electrical fuse (eFuse) one-time programmable (OTP) memory intellectual property (IP) to trim analog circuits or set initial values of digital registers. In this paper, a 128-bit eFuse OTP IP was designed using only 3.3V medium voltage (MV) devices, without the use of 1.8V low-voltage (LV) logic devices. The eFuse OTP IP, designed with 3.3V single MOS devices, can reduce the total process cost of three masks, which include the gate oxide mask of a 1.8V LV device and the LDD implant masks of NMOS and PMOS. Additionally, since the 1.8V voltage regulator circuit was not required, the size of the light sensor chip can be reduced. To further reduce the number of package pins on the light sensor chip, the VPGM voltage (program voltage) was applied through the VPGM pad during the wafer testing, and the VDD voltage was applied through the PMOS power switching circuit after packaging resulting in a reduced number of package pins.

Keywords

Single device
Light sensor
Electrical fuse (eFuse)
One-time programmable (OTP)
Program voltage

1. Introduction

A light sensor measures the brightness of the environment and automatically adjusts the screen's brightness accordingly [1]. In recent smartphones, under-panel sensor (UPS) technology is used to position the light sensor behind the display. Mobile-oriented under-display light sensors require a small non-volatile memory intellectual property (IP) known as electrical fuse one-time programmable (eFuse OTP) memory, typically with a capacity of about 128 bits. This memory is primarily utilized for trimming analog circuits and setting initial values for digital registers [2,3]. Furthermore, if the eFuse OTP IP is designed using 3.3V medium voltage (MV) devices, which are commonly used in analog circuits, instead of 1.8V low voltage (LV) devices used in digital integrated circuits, the number of masks related to LV devices can be reduced, consequently lowering production costs.

As a result, this paper presents the design of a 128-bit eFuse OTP IP that employed 3.3V MV devices, without relying on 1.8V LV devices, in a 0.18 µm complementary metal-oxide semiconductor (CMOS) image sensor (CIS) process. To accomplish this, word line (WL) driving circuits, source line (SL) driving circuits, and sense amplifier (S/A) circuits were introduced. To further decrease the number of package pins for the light sensor, a new circuit was proposed. This circuit applied the program voltage (VPGM) of 4.6V, exclusively in program mode through the VPGM pad and utilized the p-channel metal-oxide-semiconductor (PMOS) power switch circuit to apply VDD of 3.3 V in normal read mode and program-verify-read mode. Implementing this circuit in the 128-bit eFuse OTP IP reduces the process cost by eliminating the gate oxide mask for the LV device and three masks for the NMOS and PMOS lightly doped drain (LDD) implantation. Additionally, the exclusion of the 1.8V voltage regulator circuit resulted in a reduced chip area, ensuring cost competitiveness.

2. Circuit design

The circuit diagram of the eFuse OTP cell used for the design of the 128-bit eFuse OTP IP is shown in **Figure 1(a)**. A dual-port eFuse OTP cell was used [4-6], enabling the flow of minimal current through unprogrammed eFuse in read mode, employing a read-only N-channel metal-oxide semiconductor (NMOS) transistor (MN1). In program mode, a program-only NMOS transistor (MN2) was utilized to allow significant program currents to pass through the selected eFuse link. The NMOS W/L for MN1 and MN2 in **Figure 1(a)** were 0.89 µm / 0.35 µm and 180 µm / 0.35 µm, respectively. The eFuse link in the dual-port eFuse OTP cell was fabricated using n+ poly. The layout size of the designed eFuse OTP cell was 29.71 µm × 8.37 µm (248.6727 μm^2).

Table 1 shows the bias voltages at the eFuse OTP cell nodes for different operation modes in the 128-bit eFuse OTP IP. In program mode, the selected write word line (WWL) was activated at a program voltage (VPGM) of 4.6V. Unselected WWLs in the eFuse OTP IP were held at 0 V, isolating the eFuse link from the barrel (BL), and preventing current flows. To program an eFuse OTP cell in program mode, VDD voltage was applied to the input data (D_{IN}) logic '1,' and a high pulse was applied to the input control signal PGM. As a result, a VPGM of 4.6 V was applied to SL and WWL, allowing a substantial program current flow through the eFuse link and MN2. This action caused the eFuse link to blow due to thermal rupture, resulting in a resistance of tens of kΩ or more [7]. For unprogrammed cells, D_{IN} was set to 0 V, and SL was maintained at 0 V, causing no current to flow through the eFuse link, and the resistance remained unchanged. **Figure 2** illustrates the voltages of RWL, WWL, and SL in the eFuse OTP cell for program mode, based on row selection and

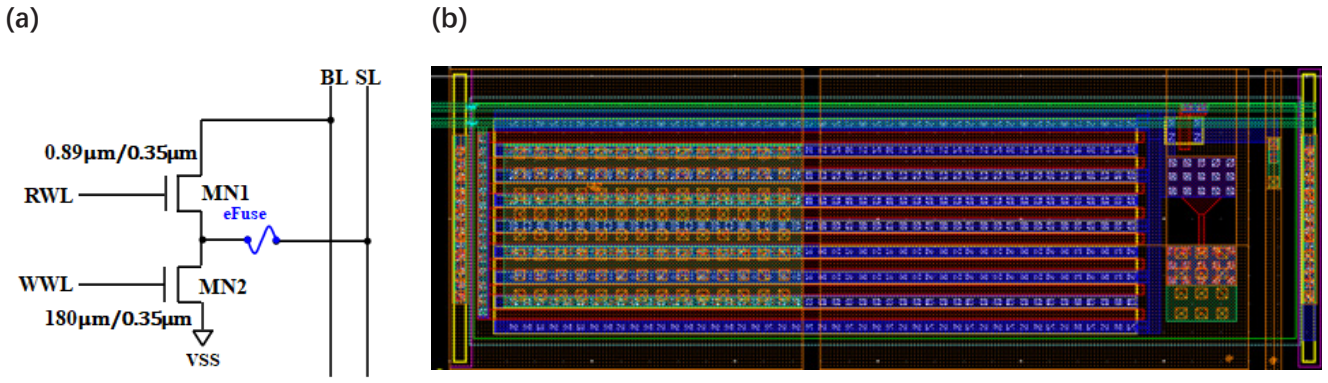

Figure 1. Dual-port eFuse OTP cell: **(a)** schematic; and **(b)** layout images

D_{IN} data. Cells with blown eFuse links in the designed eFuse OTP IP were located in the selected rows, as shown in **Figure 2**, when digital logic '1' was applied to D_{IN}. Conversely, unblown eFuse links represent unprogrammed cells, either in unselected rows or selected rows with digital logic '0' applied to D_{IN}. In read mode, only the selected RWL out of 8 (2^3) based on the decoding of row address RA [2:0] was activated with VDD voltage. For unprogrammed eFuse links, MN2 in **Figure 1(a)** provided a current path through the eFuse link, causing BL to discharge to 0 V, resulting in a digital logic '0' output at D_{OUT}. Programmed cells maintained a high-resistance state of the eFuse link, and BL voltage remained precharged to VDD, resulting in a digital logic '1' output at D_{OUT} [7].

The main characteristics of the 128-bit eFuse OTP

Table 1. Table of eFuse OTP cell bias conditions by operating mode

	Program mode		Read mode	
WWL	4.6 V		0 V	
RWL	0		VDD	
D_{IN}	0	1	×	×
SL	0	4.6 V	0	0
BL	Floating	Floating	0	VDD
D_{OUT}	×	×	0	1
eFuse	Unblown	Blown	Unblown	Blown

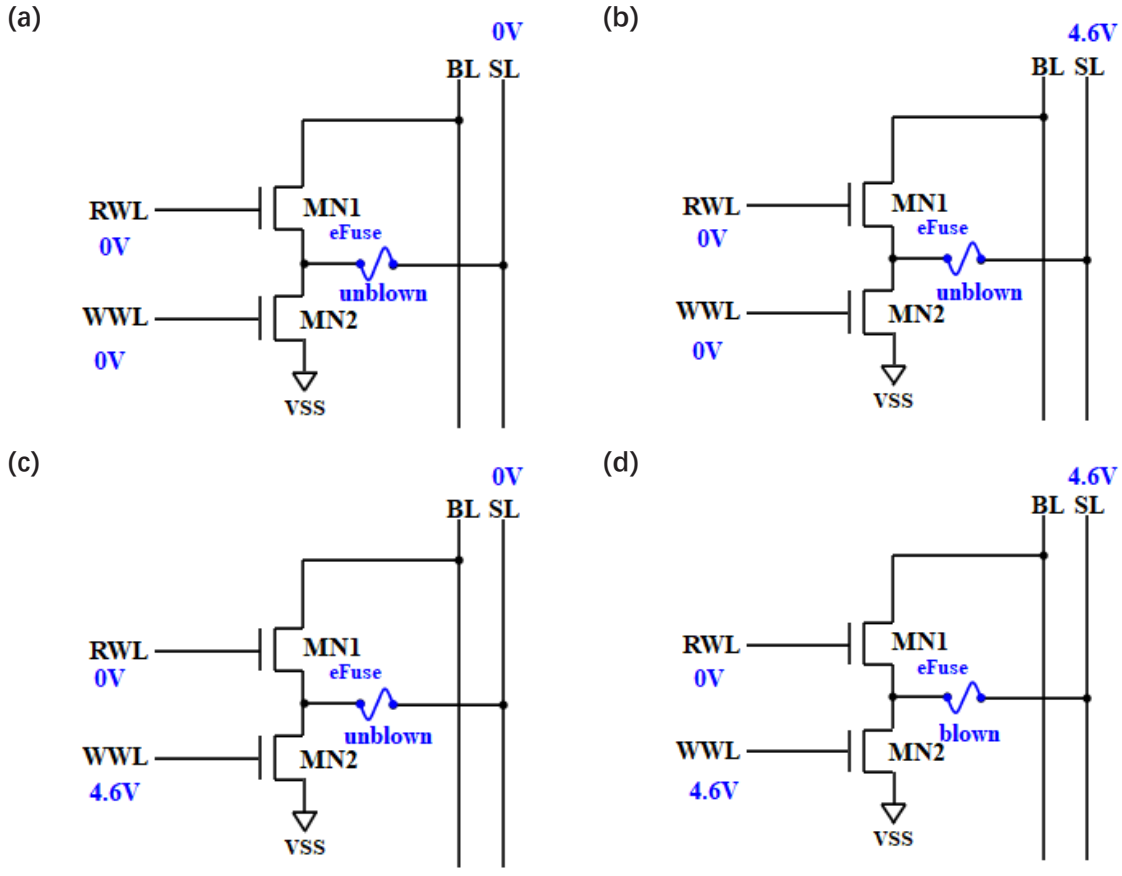

Figure 2. The voltages of RWL, WWL, and SL in eFuse OTP cell according to the row selection and D_{IN} data in the case of program mode: **(a)** unselected row and D_{IN} is '0'; **(b)** unselected row and D_{IN} is '1'; **(c)** selected row and D_{IN} is '0'; and **(d)** selected row and D_{IN} is '1'.

IP based on the 0.18 μm CIS process are outlined in **Table 2**. The cell array was configured in an 8-row by 16-column format and employed dual-port eFuse OTP cells. The operational modes included program mode, read mode, and program-verify-read mode. The design approach for the 128-bit eFuse OTP IP excluded the use of 1.8 V logic components, opting for a design using only 3.3V components. Moreover, a new method was introduced for applying VGPM exclusively in program mode through the VPGM pad, which allowed for the application of 4.6 V program voltage to the eFuse link being programmed, thereby increasing the program power. Additionally, VPGM voltage was applied in read mode and program-verify-read mode through the PMOS switch circuit. The 128-bit eFuse OTP IP featured 1-bit program bits and 8-bit read bits, with a program time of 200 μs. The top metal for the 128-bit eFuse OTP IP was metal3. **Figure 3** illustrates the circuit diagram for the 8-row by 16-column cell array in the 128-bit eFuse OTP IP, with RWL and WWL routed in the row direction, and BL and SL routed in the column direction.

In this paper, to reduce the number of package pins for the light sensor when applied to the light sensor, a new circuit was proposed for applying VPGM voltage only through the VPGM pad in program mode during the wafer testing, and for applying VDD of 3.3 V

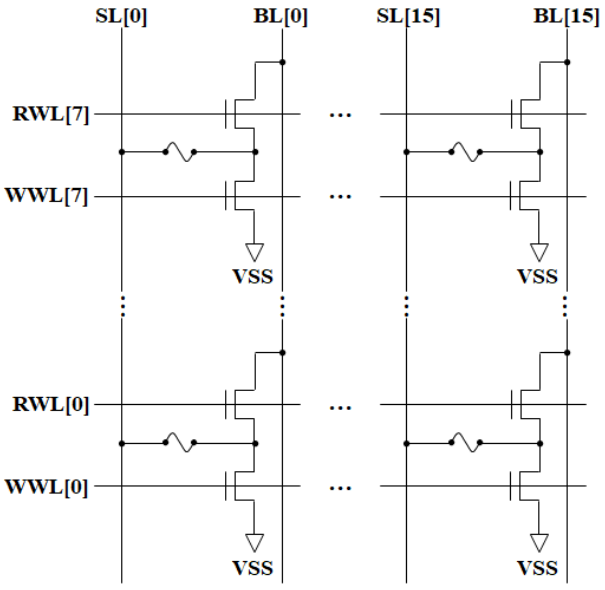

Figure 3. Cell array of 8 rows × 16 columns

through the PMOS power switch circuit in the read mode and program-verify-read mode. Therefore, the designed eFuse OTP IP had VPGM voltage applied through the VPGM pad during wafer testing, with 4.6 V voltage, and after packaging, the VPGM pad was kept floating, making it equivalent to 0 V. **Figure 4** illustrates the power switching circuit proposed in this paper. In program mode, the PWSW_EN signal was set to 0 V, and VDD and VPGM voltages were applied as 3.3 V and 4.6 V, respectively. In **Figure 4**, the cross-

Table 2. Major features of the designed 128-bit eFuse OTP IP

Items		**Main features**
Process		DBH 0.18 μm CIS process
OTP cell array		8R × 16C
VDD	Read	1.61 V – 3.60 V
	Program	3.00 V – 3.60 V
	Program-verify-read	1.62 V – 3.60 V
VPGM	Read	Floating
	Program	4.6 V
	Program-verify-read	Floating
Operating mode		Program / Read / Program-verify-read
Program bit / read bit		1 bit / 16 bit
Program time		200 μs
Top metal		M3

coupled PMOS transistors, MP3 and MP4, were in OFF and ON states, respectively, biasing the N3 node voltage to 4.6 V, which in turn set the N1 and N2 node voltages to 4.6 V and VDD voltages during program mode, turning off both PMOS transistors MP3 and MP4. On the other hand, in read mode and program-verify-read mode, PWSW_EN was set to VDD, and both VDD and VPGM voltages were set to 3.3 V and floating, respectively. Under these conditions, MP3 and MP4 were in ON and OFF states, respectively, so the N3 node voltage became VDD. At this point, both N1 and N2 voltages became 0 V, turning on the PMOS transistors MP1 and MP2, providing VDD voltage to the floating VPGM voltage in **Figure 5**'s row drive circuit and **Figure 6**'s SL drive circuit, making use of the VPGM voltage as the switching power.

Figure 5's row drive circuit selected one out of eight rows based on the decoding of row address RA [3:0]. **Figure 6**'s SL drive circuit, on the other hand, selected one out of 16 SL drive circuits based on the decoding of column address CA [2:0] in program mode. The SL drive circuit operated by supplying 4.6 V program voltage to the selected SL when the digital logic of D_{IN} is '1,' and it drove the selected SL to 0 V when the digital logic of D_{IN} is '0.' In read mode and program-verify-read mode, the IPGM signal was in a digital logic '0' state, ensuring that all 16 SL drive circuits always operated at 0 V. In the conventional row drive circuit and SL drive circuit, the components within the dashed-dotted boxes were designed using 1.8 V logic components. However, in this paper, these components in the designed circuit were replaced with 3.3 V components instead of 1.8 V components, as highlighted within the dashed-dotted boxes in **Figures 5** and **6**.

In the eFuse OTP IP, if the precharge voltage of BL to VDD was applied in the BL S/A, it may lead to the blowing of unprogrammed eFuse links [8]. Therefore, in this paper, the VSS precharge method for BL S/A circuits is shown in **Figure 7** [8], where the precharge voltage of BL was changed from VDD to VSS. In the

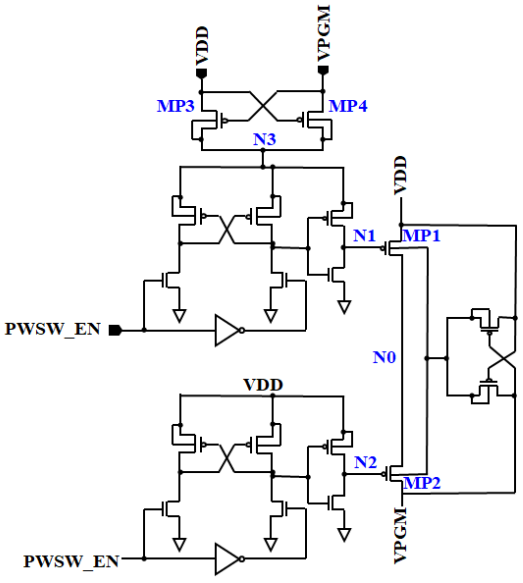

Figure 4. Proposed power switching circuit

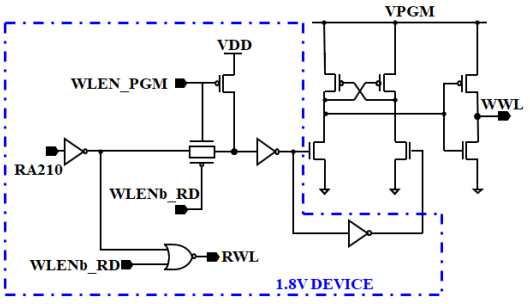

Figure 5. Row driver

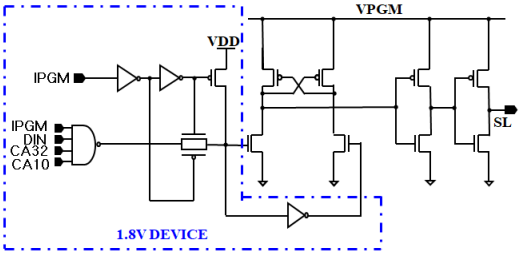

Figure 6. SL driver

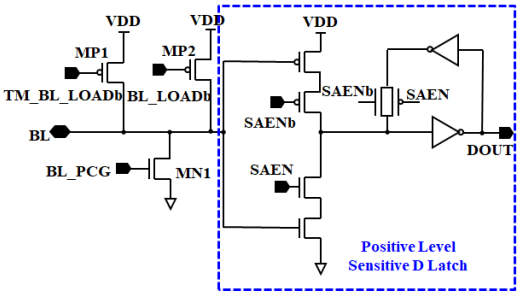

Figure 7. BL S/A circuit

BL S/A circuit (**Figure 7**) used in this paper, before the activation of the RWL signal in read mode and program-verify-read mode, the NMOS transistor MN1 precharged the BL voltage to VSS. Therefore, only when reading programmed eFuse OTP cells, the BL voltage was pulled up to VDD when a low pulse was generated on the BL_LOADb signal, while in the case of unprogrammed eFuse OTP cells, it maintained the VSS precharge voltage before the activation of RWL. BL data was latched by a positive-level-sensitive D-latch circuit using the sense amplifier enable signal (SAEN) as a clock.

Additionally, the BL S/A circuit in **Figure 7** was designed considering the resistance variation of programmed eFuse links over a data retention time of 10 years. After programming the eFuse links, in program-verify-read mode, the PMOS transistor in **Figure 7** was turned on to test whether the eFuse resistance has been programmed correctly to be above 10 kΩ. In the read mode, as used in actual applications, only the MP2 in **Figure 7** was turned on to reduce the pull-up resistance, allowing the BL voltage to be sensed as normal '1' data if the eFuse resistance was maintained above 5 kΩ. In this manner, a variable BL pull-up load method was adopted [8], which varied the BL pull-up load used in the BL S/A circuit depending on the program-verify-read mode and read mode. Moreover, the BL S/A circuit in **Figure 7** was designed using 3.3 V components instead of 1.8 V logic components.

By designing the eFuse OTP cell and its surrounding circuits using only 3.3 V MOS components, the light sensor chip utilizing the 128-bit eFuse OTP IP can reduce the process cost by eliminating a total of three masks related to the gate oxide mask as well as NMOS and PMOS LDD implant masks, which are associated with LV components. When both 1.8 V and 3.3 V power supplies were used, a 1.8 V voltage regulator circuit was required to regulate 3.3 V to 1.8 V for supplying power. However, in the design proposed in this paper using 3.3 V single components, the 1.8 V voltage regulator circuit can be excluded. Consequently, this reduced the chip's footprint, ensuring cost competitiveness.

3. Simulation and layout results

Figure 8 illustrates the voltage waveforms of the designed 128-bit eFuse OTP IP under simulated conditions with VDD of 1.62 V, slow NMOS slow PMOS (SS) model parameters, and temperature of 85°C, using the 0.18 μm CMOS image sensor process. In **Figure 8**, the *x*-axis represents time, and the *y*-axis shows the voltage waveforms of input signals in the power switching circuit from **Figure 4**, including the PWSW_EN signal, VPGM voltage, internal node voltages (N0, N1, and N2) in the power switching circuit, and the voltage waveform of the program input signal PGM in the eFuse OTP IP. As depicted in **Figure 8**, after applying 0 V to the PWSE_EN signal from VDD of 1.62V, and then applying 4.6 V through the VPGM pad, the N1 node voltage at the gate of MP1 transistor in **Figure 4** reached 4.6 V, turning off the MP1 transistor. Simultaneously, when the PWSW_EN voltage in **Figure 8** dropped from VDD voltage to 0 V, the N2 node voltage at the gate of the MP2 transistor in **Figure 4** switched from 0 V to VDD voltage, turning the MP2 PMOS transistor on. Looking at the power

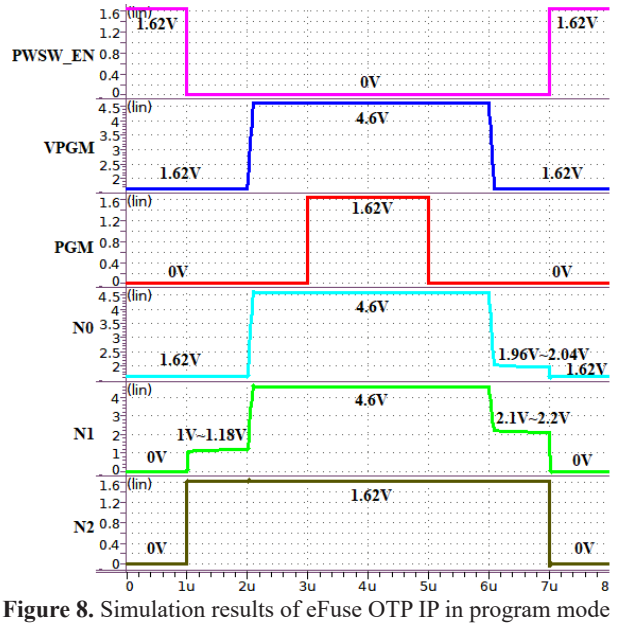

Figure 8. Simulation results of eFuse OTP IP in program mode

Table 3. Simulation results for eFuse sensing resistor programmed in 128-bit eFuse OTP IP

Operation mode	Temp	SS model	SF model	TT model	FS model	FF model
PVR	-40°C	5.9 K	3.2 K	5.9 K	9.3 K	5.7 K
	25°C	6.7 K	3.8 K	6.5 K	9.8 K	6.3 K
	85°C	7.3 K	4.3 K	7.1 K	10.0 K	6.7 K
Read	-40°C	2.5 K	0.9 K	2.6 K	4.9 K	2.7 K
	25°C	2.6 K	1.0 K	2.8 K	5.0 K	2.9 K
	85°C	2.8 K	1.1 K	2.9 K	4.9 K	2.9 K

switching circuit, as the PWSW_EN signal fell from VDD to 0 V, in the proposed power switching circuit in **Figure 4**, MP2 turned on while MP1 turned off, preventing a short circuit between VDD voltage and VPGM voltage.

Table 3 presents the simulation results for the sensed resistance of programmed eFuse in a 128-bit eFuse OTP IP employing the variable BL pull-up load method, which varied with program-verify-read mode and read mode, under the condition of VDD at 1.62 V, MOS model parameters, and temperature fluctuations. As shown in **Table 3**, in the program-verify-read mode and read mode, the sensed resistance of the programmed eFuse is 10 kΩ and 5 kΩ, respectively.

Figure 9 shows the layout image of the 128-bit eFuse OTP IP designed for use in a light sensor, using the 0.18 μm CMOS image sensor process. The layout size of the 128-bit eFuse OTP IP was 278.725 μm × 249.98 μm (0.0697 mm^2). The designed 128-bit eFuse OTP IP has been applied to an actual light sensor chip, and its basic functionality has been confirmed through wafer testing and package testing.

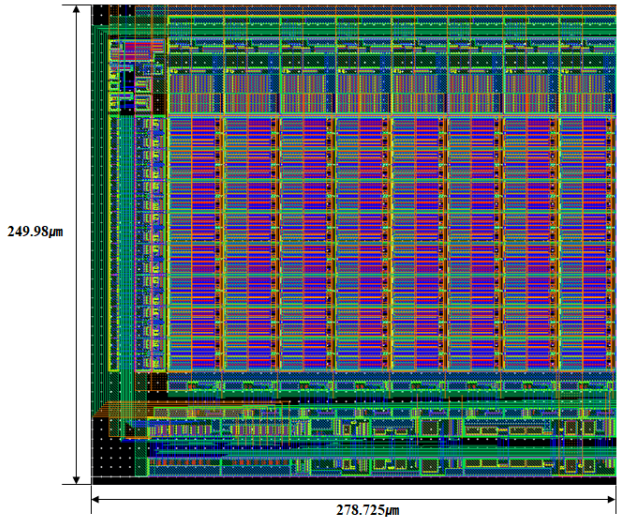

Figure 9. Layout image of the designed 128-bit eFuse OTP IP

4. Conclusion

Light sensor chips require non-volatile memory IP, specifically eFuse OTP memory IP, for trimming analog circuits and setting initial values of digital registers.

In this paper, a 128-bit eFuse OTP IP was designed using the 0.18 μm CIS process without the use of 1.8 V logic devices, opting for 3.3 V MV devices instead. The designed 128-bit eFuse OTP IP encompasses core circuits, including row drive circuits, SL drive circuits, and BL S/A, all designed with 3.3 V single MOS devices. By designing the 128-bit eFuse OTP IP with only 3.3 V MOS devices, the process cost of three masks, including the gate oxide mask of the 1.8 V LV device and the LDD implant mask of NMOS and PMOS, can be reduced. Furthermore, by excluding the 1.8 V voltage regulator circuit, the chip size was reduced, ensuring cost-effectiveness. To minimize the number of package pins for the light sensor chip, a new circuit that applied the program voltage VPGM only through the VPGM pad during the wafer testing was proposed, and the VDD voltage was supplied through the PMOS power switching circuit after packaging, reducing the number of package pins. While the disadvantage of this approach is the inability to program in the packaged state, the benefit of reducing

the pint count becomes crucial in certain cases. From a layout perspective, using 3.3 V devices instead of 1.8 V devices in the surrounding circuits of the 128-bit eFuse OTP IP did not increase IP size as no additional routing channels were needed.

The layout size of the designed 128-bit eFuse OTP IP was 278.725 μm × 249.98 μm (0.0698 mm^2). It has been applied to a light sensor chip, and its basic functionality has been confirmed through wafer testing and package testing.

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Disclosure statement

The authors declare no conflict of interest.

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