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Determining Optimal Ion Implantation Conditions to Prevent Double Snapback in High-Voltage Electrostatic Protection DDDNMOS Devices

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Abstract

Process and device simulations were performed to determine the optimal ion implantation conditions to prevent double snapback of high voltage operating DDDNMOS (double diffused drain N-type MOSFET) device for electrostatic discharge (ESD) protection. By examining the effects of HP-Well, N^- drift and N^+ drain ion implantation on the double snapback and avalanche breakdown voltages, it was possible to prevent double snapback and improve the electrostatic protection performance. Optimizing the ion implantation concentration in the N^- drift region rather than the HP-Well region prevents the transition from the primary on-state to the secondary on-state, leading to improved ESD protection performance. As the concentration of the N^- drift region affects both leakage current and avalanche breakdown voltage, for process technologies operating with voltages exceeding 30V, implementing new structures like DPS or optimizing process conditions can result in improved ESD protection performance.

Keywords

ESD (electrostatic discharge)
DDDNMOS (double diffused drain N-type MOSFET)
Double snapback
V_{av} (avalanche breakdown voltage)
Design window
Simulation
DPS (double polarity source)
Colligation

1. Introduction

With the development of semiconductor process technology and the ultra-high integration of integrated circuits (ICs), electrostatic discharge (ESD) has become an important factor affecting productivity, product stability, and overall reliability. In the semiconductor industry, advances in process technology and the miniaturization and ultra-high integration of ICs have led to improvements in circuit performance and speed. However, malfunction and destruction of circuits due to ESD have become a significant problem. The significance of ESD protection circuits is increasing, leading to active research on ESD protection devices. When ESD occurs in microchips for display driving that

operate at high voltage, the performance of microchips such as LCD driver IC (LDI) and Display Driver IC (DDIC) can degrade due to problems such as malfunction and physical damage of the electronic device. Therefore, various MOSFET structures have been introduced to ensure reliable ESD protection [1,2]. One of the basic requirements for a MOSFET device is that the avalanche breakdown voltage (V_{av}) must be higher than the operating voltage (Vop). For N-type MOSFET devices operating at high voltage, double diffused drain N-type MOS (DDDNMOS) has generally been used as the basic device to satisfy the above characteristics [1,2]. However, analyses of the transmission line pulse (TLP) test I-V characteristics of DDDNMOS devices adopted to date have revealed the following problems [3,4]. (i) Firstly, double snapback occurs. The first snapback is weak, while the second snapback is strong, where the snapback holding voltage is much smaller than the operating voltage. Secondly, as the operating voltage increases, the secondary ON state predominates, and as the operating voltage decreases, the primary ON state predominates. When the primary ON state is dominant, relatively good electrostatic protection performance is obtained, i.e., linearity of the current immunity level with respect to active width/finger number. However, when the secondary on state is the dominant ON state, the I-V characteristics are very unstable, i.e., sensitive to changes in process variables and design parameters, and lack reproducibility and consistency.

Therefore, in this paper, the mechanism of double snapback occurrence, especially the mechanism related to the transition from the primary ON state to the secondary ON state were investigated through process and device simulations. Furthermore, by extracting the critical process parameters that determine the transition from the primary on to the secondary on state among various process variables (HP-well, N^- drift and N^+ drain ion implantation), we aim to explore how DDDNMOS devices operating at high voltages can be prevented from transitioning to the secondary on state in the high-current region and achieve good electrostatic protection. By applying the obtained optimal ion implantation conditions to actual device fabrication, we aim to improve the electrostatic protection performance by preventing double snapback.

2. Determination of design parameters through the design window

In order for an electrostatic protection circuit to operate normally under bi-directional electrostatic stress, each electrostatic protection element in the microchip must have a forward diode behavior and an avalanche breakdown snapback behavior depending on the direction of the stress applied [5]. **Figure 1** is a design window showing the I-V characteristics of an electrostatic protector, which was used to determine the design parameters shown in **Table 1** [5,6]. The I-V characteristics of an electrostatic protector shown in Figure 1 are turned off when the circuit is under normal conditions ($0 \preceq$ Voltage $\preceq V_{op}$) and turned on only under abnormal conditions such as electrostatic stress. In addition to the double snapback phenomenon, the nonlinearity of the current immunity level with changes in the internal spread width or number of fingers is also a problem that hinders the performance of electrostatic protection [6]. In general, the linearity of the current immunity level of an electrostatic protective device is guaranteed when the thermal breakdown voltage (V_{t2}) is greater than the triggering voltage (V_{t1}). The necessary and sufficient conditions for electrostatic protection to satisfy the above design window are shown in **Table 1** [6].

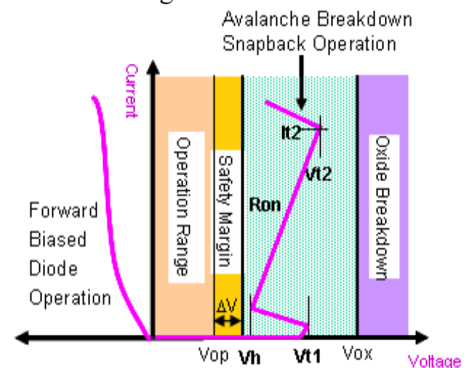


Figure 1. Design window of ESD protection device. Abbreviations: V_{op}, operation voltage; V_{ox}, gate oxide breakdown voltage); V_h, snapback holding voltage; V_{t1}, triggering voltage; V_{t2}, thermal breakdownvoltage; I_{tb}, thermal breakdown current; R_{on}, on resistance = slope of graph; ΔV, safety margin).

Table 1. Requirements for ESD protection

Requirements for ESD protection
$V_{op} < V_{av}, V_{t1}$ $V_{t1}, V_{t2} < V_{ox}$ $V_{op} + \Delta V < V_h$ I_{tb} : Large $V_{t1} \le V_{t2}$

3. Device structure and simulation method

3.1. Device structure

Figure 2 shows a schematic cross-section of a DDDNMOS device, which uses a structure with a double diffusion drain (DDD) that surrounds the N^+ drain region with an N-drift diffusion region. The device is designed so that the gate and N^+ drain regions are not adjacent to each other. For MOSFET devices operating under electrostatic stress, the background doping concentration (BDC), which is the concentration in the junction region (N^- drift/HP-well) indicated by the right circle in **Figure 2**, plays a very important role in satisfying the condition that V_{av} must be greater than V_{op}, as shown in **Table 1** [7]. Since V_{av} is determined by the concentration of impurities in the two regions with opposite polarity, the V_{av} of an NMOS device with DDD structure is determined by the lateral breakdown voltage of the N^- drift/HP-well junction, which in turn is determined by the amount of ion injection into the N^- drift region and the HP-well region. In general, the lower the impurity concentration in the two regions, the higher the V_{av} tends to be. Therefore, by adopting a DDD structure, the impurity concentration in the drift region in contact with the HP-well region can be sufficiently reduced to obtain a high V_{av} value of the target size. **Table 2** summarizes the typical process conditions used to fabricate DDDMOS devices. The N^+ drain region was ionized at a high dose of ~1015 $cm^{-2,}$ while the N^- drift region surrounding the drain was ionized at a relatively low dose of ~1013 cm^{-2}. In addition, the channel-forming HP-well region was ionized at a lower dose than the drift region in the range of ~1012 cm^{-2}.

Table 2. Typical process conditions for DDDNMOS standard devices

Process Name	Process Condition
HP-well implant	B, 300KeV, $7.5\times10^{12}cm^{-2}$
Well drive-in	1,200℃, 30min
N^- drift implant	P, 80KeV, $1.1\times10^{13}cm^{-2}$
N^- Drift dive-in	1,100℃, 60min
HNF implant	B, 180KeV, $8.5\times10^{13}cm^{-2}$
HPF implant	P, 500KeV, $1.6\times10^{13}cm^{-2}$
Thick gate oxidation	850℃, 75min, (120Å)
Thin gate oxidation	850℃, 33min, (30Å)
N^+ active implant	As, 60KeV, $5.0\times10^{15}cm^{-2}$ P, 30KeV, $3.0\times10^{13}cm^{-2}$
P^+ active implant	BF2, 25KeV, $3.0\times10^{15}cm^{-2}$ B, 30KeV, $2.0\times10^{13}cm^{-2}$
S/D anneal	600℃, 1min, RTP

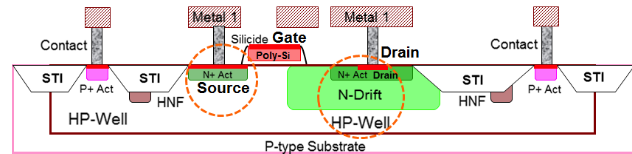


Figure 2. Cross-sectional schematic diagram of DDDNMOS device

3.2. Simulation methods

The structure of the DDDNMOS device was formed using the TMA process simulation tool (TSUPREM-4), and the process simulation conditions were based on the 0.18μm _30V standard process. The formed device structure was input into the input file of the ISE tool to perform mesh optimization (mDraw), followed by device simulation (DESSIS). The high-current characteristics of the DDDNMOS device were analyzed by performing two-dimensional simulations with built-in thermal characteristics, and mixed mode transient (MMT) simulations were performed by applying trapezoidal current pulses with a rise time of 10 ns and a duration of 100 ns to simulate the electrostatic stress

of a human body model (HBM). To investigate the effect of ion implantation conditions on the double snapback phenomenon, dozens of iterative simulations by 2D matrix combination were performed to determine the optimal ion implantation range by varying the ion implantation amount in the HP-well, N^- drift, and N^+ drain, respectively. The robustness and high current characteristics of the fabricated DDDNMOS devices were analyzed using a TLP measurement system (Barth 4002) [8].

4. Simulation results

4.1. Simulation comparison with I-V TLP data

Figure 3 shows a comparison of the simulated and TLPI-V characteristics of the DDDNMOS device. The characteristics such as avalanche breakdown, double snapback, and low secondary snapback voltage showed that the TLP data and simulation results tend to be in qualitative agreement. In particular, the double snapback phenomenon and the resulting characteristics of the primary ON and secondary ON states were clearly consistent with the simulation results. In particular, the slope of the current-temperature curve clearly changed when the primary ON state transitioned to the secondary ON state, indicating that the conduction mechanism inside the device is fundamentally different.

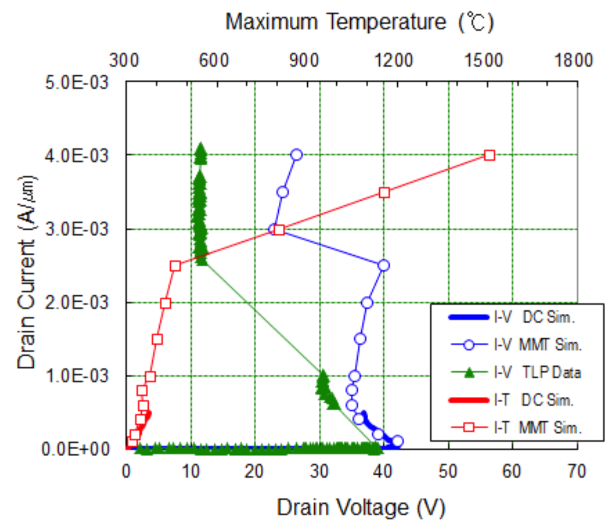


Figure 3. Comparison of simulation and TLP I-V characteristics of DDDNMOS standard device

4.2. Analysis of double snapback and thermal breakdown mechanism by contour analysis

In order to analyze the double snapback and thermal breakdown mechanisms observed in the DDDNMOS standard device, **Figure 4** shows the contour data of the current density, total current, electric field, and maximum temperature in the primary on state and secondary on state in order to consider the double snapback and thermal breakdown mechanisms. The results showed that the direct cause of the double snapback was due to the formation of a deep electron channel under the gate. As the current increased, the electron-rich region from the source to the drain gradually expanded, and when the current was above a certain threshold, a deep channel was formed under the gate in the electron-rich region connecting the source and drain, which was the mechanism for the device to transition from the first ON state to the second ON state. In addition, the field localization played an important role in the thermal breakdown. The field, which was evenly distributed throughout the drift region before

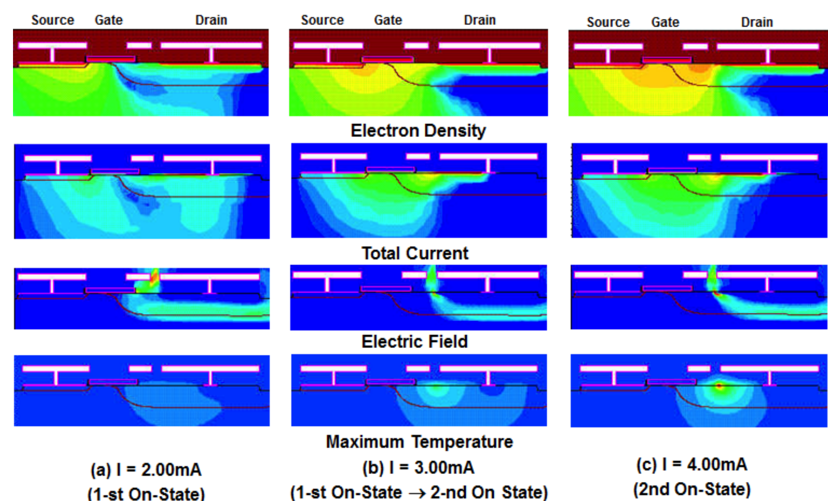


Figure 4. Contour distribution for current density, total current, electric field and maximum temperature

the formation of the electron channel, was concentrated in the N^+ drain and N^- drift/surface regions as the deep electron channel was formed, which resulted in a sharp increase in temperature in those regions, which was the mechanism by which thermal breakdown occurred.

4.3. Effect of process parameters

The effects of HP-well ion implantation, drift ion implantation, and active ion implantation on the I-V characteristics in the high current region of DDDNMOS were analyzed.

4.3.1. Effect of HP-well ion implantation volume

Figure 5 shows the simulated and TLP I-V characteristics as a function of HP-well ionization. The results showed that double snapback occurred regardless of the well ionization volume, which means that the well ionization volume does not fundamentally change the conduction mechanism in the high current region. In addition, the primary ON state of the TLP I-V curve in the high-current region shrank, the secondary ON state expanded, and the ionization volume increased. V_h and R_{on} decreased and I_{tb} increased with increasing well ionization. The contour data did not change significantly with the change in ionization of the well.

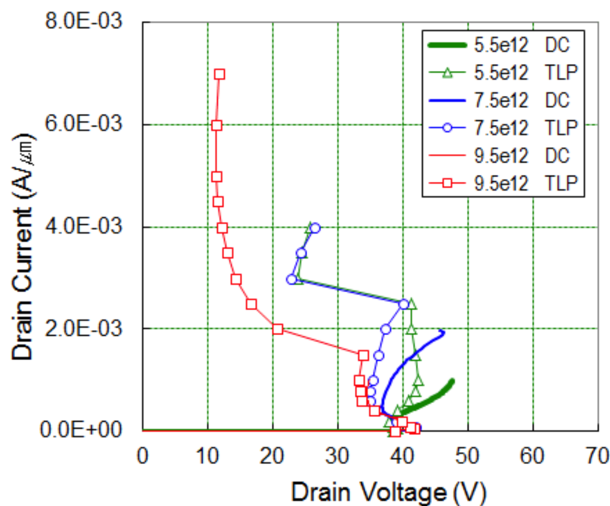


Figure 5. Comparison of simulation and TLP I-V characteristics according to well implant dose

4.3.2. Influence of N^- drift ionization volume

Figure 6 shows the simulated and TLP I-V characteristics as a function of N^- drift ionization volume. The leakage current tends to increase and V_{av} decreases as the drift ionization dose increases. It can be seen that the drift ionization rate is an important factor in determining whether double snapback occurs, i.e., if the drift ionization rate is kept above a certain threshold, good electrostatic protection can be achieved even in the high-current region because no deep channel is formed under the gate and the transition from the first ON state to the second ON state cannot occur. If the drift ionization rate is less than or equal to 1.1 × 1013cm^{-2}, double snapback occurs when the total current reaches the threshold value, as a deep electronic channel is formed at the bottom of the gate. On the other hand, if the drift ion injection amount is above 3.3 × 1013 cm^{-2}, double snapback does not occur because no electronic channel is formed under the gate even if the total current increases, so the first ON state is maintained until thermal breakdown occurs.

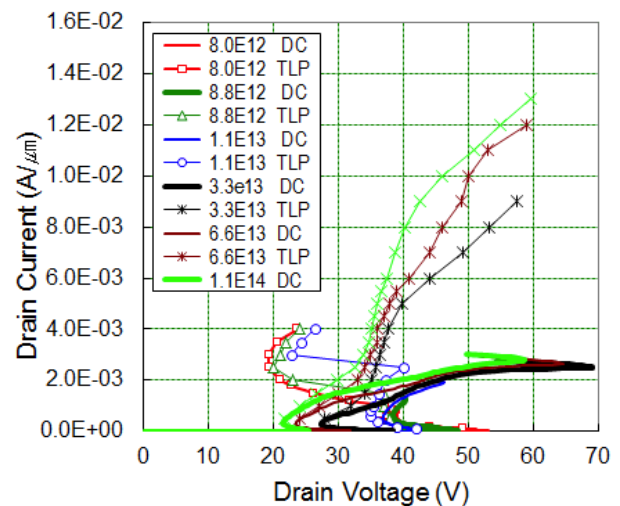
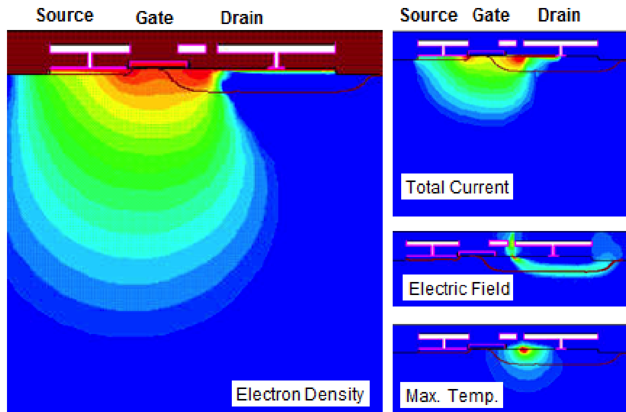
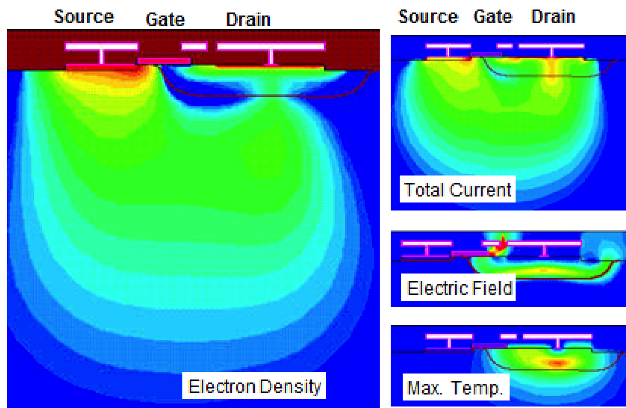


Figure 6. Comparison of simulation and TLP I-V characteristics according to drift implant dose

Figure 7 shows the contour distribution as the drift ionization dose changes. The current was not concentrated on the surface of the device but remained constant in the depth direction, and the lateral field



(a) Drift dose = 8.0 × 10^{12}cm^{-2}, Current = 3.5 mA/um



(b) Drift dose = 3.3 × 10^{13}cm^{-2}, Current = 8.0 mA/um

Figure 7. Contour distribution according to drift implant dose.

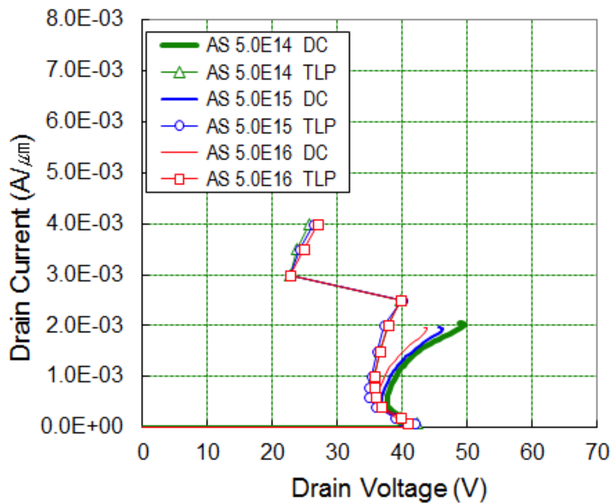


Figure 8. Comparison of simulation and TLP I-V characteristics according to source/drain ion implant dose

remained uniform and broad in the initial state. Therefore, the point of thermal breakdown was also widely distributed in the region below the N^+ drain. Considering the leakage current and V_{av} depending on the drift ion injection amount, it can be predicted that a drift degree of 3.3×1013 cm^{-2} is applicable for operating voltages below 30 V.

4.3.3. Influence of active ionization volume

Figure 8 shows a comparison of simulated and TLP I-V results as the source/drain ionization volume is varied. The TLP I-V curve and contour characteristics of the DDDNMOS did not change at all when the source/drain ion implantation amount was varied within the range of 5.0 × 1014 to 5.0×1016 cm^{-2}. Therefore, this indicates that changing the ion implantation amount for the source/drain area front has no effect on the electrostatic protection performance of DDDNMOS.

4.4. Impact of incorporating process variables

In **Section 4.3**, it was explained that optimally designing the N^- drift ion implantation amount among the process parameters can prevent the device from switching from the primary on state to the secondary on state in the high current region, thus achieving very good electrostatic protection performance. However, while increasing the amount of N-drift ion implantation can prevent double snapback of the device, the problem is that it cannot be applied to operating voltages greater than 30V due to the relatively lower V_{av} value. Therefore, to prevent the transition to the secondary on state while maintaining the desired V_{av} value, an alternative is to change the ionization conditions or structure of the source while maintaining the well/drift/active ionization conditions. In other words, if a P^+ diffusion layer formed by adding P^+ ion implantation right next to the N^+ source is placed between the existing N^+ source and the N^+ drain, it can impede the flow of electrons from the N^+ source and thus prevent the development of an electron channel downstream of the gate, forcing the device to remain in the primary ON

state until thermal breakdown occurs. Simulations of a device with a double polarity source (DPS) in the above form have shown that V_{av} is the same as that of a standard device, but with improved electrostatic protection that prevents double snapback [9]. The contour distribution also shows that the field is distributed without forming an electronic channel until thermal breakdown occurs. DDDNMOS with DPS structure can achieve improved electrostatic protection performance compared to standard devices. Optimizing the size of the added P^+ diffusion region and the amount of ion implantation can reliably prevent the appearance of the electronic channel and secondary ON state. As described above, we tried to find the optimal ion implantation conditions by varying the well ion implantation amount, drift ion implantation amount, and sodium/drain ion implantation amount individually, or to prevent double snapback by changing the sodium structure to DPS [9]. Finally, since the V_{av} of the device was lowered by increasing the drift ion implantation amount. We propose the colligation condition as shown in **Table 3** to find a more effective method as an alternative to DPS. Based on the fact that the change of drift ion implantation had the largest impact on the double snapback in the optimization simulations performed separately, we investigated the effect of various process parameters such as ion implantation energy, retrograde multiple ion implantation and thermal drive-in on the double snapback when applied in collaboration as shown in **Table 3**.

Table 3. Suggestion of colligation conditions

Process Name	Process Condition
N^- Drift Implant	P, 80KeV, $1.1\times10^{13}cm^{-2}$ P, 80KeV, $3.3\times0^{13}cm^{-2}$
Drift drive-in	1,100℃, 60min
⇩	⇩
Colligation of multiple implant (energy, multiple implant conditions)	P, 700KeV, $7.0\times10^{12}cm^{-2}$ P, 200KeV, $6.0\times10^{12}cm^{-2}$ P, 160KeV, $2.0\times10^{12}cm^{-2}$ As, 140KeV, $8.0\times10^{12}cm^{-2}$
Drift drive-in	1,100℃, 60min

Figure 9 compares the I-V characteristics as a function of ion implantation energy, retrograde multiple ion implantation, and drive-in conditions, and shows that the drift ion implantation of 3.3 × 1013 cm^{-2} has better snapback characteristics than the drift ion implantation case. This is thought to be due to the fact that applying different ion injection energies in the drift ion injection process to retrograde multiple ion injections while simultaneously applying a weaker thermal drive-in resulted in the same result, i.e., a further increase in the drift ion injection volume. However, the Vav is caused by the same mechanism, i.e., electron channeling and field localization, as the 0.18 µm_30 V DDDNMOS standard device (@ drift dose = 1.1×1013 cm^{-2}), suggesting that it is somewhat limited. In the future, a more comprehensive analysis of the integration of various process variables may lead to improved electrostatic properties.

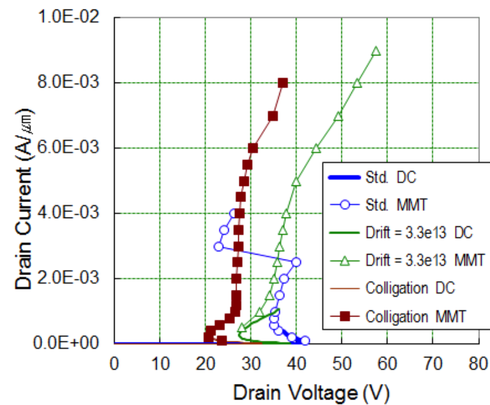


Figure 9. Comparison of I-V characteristics according to the change of colligation conditions. (ion implant energy, retrograde multiple ion implant, and drive-in)

5. Conclusion

DDDNMOS devices for high voltage formed a deep electron channel under the gate by an electron-rich region extending from the source to the drain side in the high current region. The effect is a double snapback, i.e., a transition from the primary ON state to the secondary ON state. When a DDDNMOS device transitions to the secondary on state, it exhibits very unstable I-V characteristics, which makes it impossible to achieve stable electrostatic protection performance.

In order to improve the unstable electrostatic protection performance of DDDNMOS, process and device simulations were conducted, and it was found that among various process parameters, the drift ion injection amount is an important critical factor that can control the double snapback occurring in DDDNMOS devices, i.e., the drift ion injection amount can be increased to 3.3 × 1013 cm^{-2} or more, relatively good electrostatic protection performance was obtained by preventing the transition from the primary ON state to the secondary ON state. In addition, since the drift ion implantation concentration affects the leakage current and V_{av}, the method of maintaining the drift ion implantation concentration above 3.3 × 1013cm^{-2} can only be applied to DDDNMOS processes with an operating voltage of 30 V or less. For technologies with operating voltages greater than 30 V, electrostatic protection performance can be improved by using DDDNMOS devices with a DPS structure or, alternatively, by applying various process parameters in collaboration.

Disclosure statement

The author declares no conflict of interest.

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